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Data Sheet | December 15, 2011 | FN483.6

General Purpose NPN Transistor Array

The CA3086 consists of five general-purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially connected pair.

The transistors of the CA3086 are well suited to a wide variety of applications in low-power systems at frequencies from DC to 120MHz. They may be used as discrete transistors in conventional circuits. However, they also provide the very significant inherent advantages unique to integrated circuits, such as compactness, ease of physical handling and thermal matching.

Ordering Information

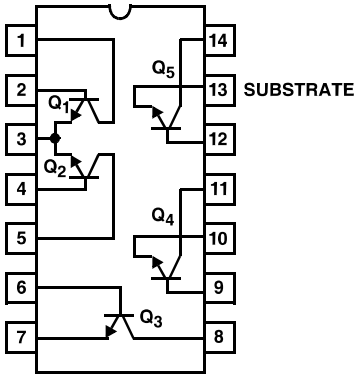
PART NUMBER (BRAND)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. DWG. #
CA3086	-55 to 125	14 Ld PDIP	E14.3
CA3086M96 (3086)	-55 to 125	14 Ld SOIC Tape and Reel	M14.15

Applications

- Power Applications from DC to 120MHz
- General-Purpose Use in Signal Processing Systems Operating in the DC to 190MHz Range
- Temperature Compensated Amplifiers
- See Application Note, AN5296 “Application of the CA3018 Integrated-Circuit Transistor Array” for Suggested Applications

Pinout

CA3086 (PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO} 15V
Collector-to-Base Voltage, V_{CBO} 20V
Collector-to-Substrate Voltage, V_{CIO} (Note 1) 20V
Emitter-to-Base Voltage, V_{EBO} 5V
Collector Current, I_C 50mA

Operating Conditions

Temperature Range . . . . . -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	110	N/A
SOIC Package	130	N/A

Maximum Power Dissipation (Any one transistor) 300mW
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor in the CA3086 is isolated from the substrate by an integral diode. The substrate (Terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action. To avoid undesirable coupling between transistors, the substrate (Terminal 13) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25^oC$, For Equipment Design

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$	20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu A$, $I_{CI} = 0$	20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$	5	7	-	V
Collector-Cutoff Current (Figure 1)	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$,	-	0.002	100	nA
Collector-Cutoff Current (Figure 2)	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$,	-	(Figure 2)	5	μA
DC Forward-Current Transfer Ratio (Figure 3)	h_{FE}	$V_{CE} = 3V$, $I_C = 1mA$	40	100	-	

Electrical Specifications $T_A = 25^oC$, Typical Values Intended Only for Design Guidance

PARAMETER	SYMBOL	TEST CONDITIONS		TYPICAL VALUES	UNITS
DC Forward-Current Transfer Ratio (Figure 3)	h_{FE}	$V_{CE} = 3V$	$I_C = 10mA$	100	
			$I_C = 10\mu A$	54	
Base-to-Emitter Voltage (Figure 4)	V_{BE}	$V_{CE} = 3V$	$I_E = 1$ mA	0.715	V
			$I_E = 10mA$	0.800	V
V_{BE} Temperature Coefficient (Figure 5)	$\Delta V_{BE}/\Delta T$	$V_{CE} = 3V$, $I_C = 1$ mA		-1.9	$mV/^oC$
Collector-to-Emitter Saturation Voltage	$V_{CE\ SAT}$	$I_B = 1mA$, $I_C = 10mA$		0.23	V
Noise Figure (Low Frequency)	NF	f = 1kHz, $V_{CE} = 3V$, $I_C = 100\mu A$, $R_S = 1k\Omega$		3.25	dB

Electrical Specifications $T_A = 25^oC$, Typical Values Intended Only for Design Guidance **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL VALUES	UNITS
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:		f = 1kHz, V_{CE} = 3V, I_C = 1mA		
Forward Current-Transfer Ratio (Figure 6)	h_{FE}		100	-
Short-Circuit Input Impedance (Figure 6)	h_{IE}		3.5	kΩ
Open-Circuit Output Impedance (Figure 6)	h_{OE}		15.6	μS
Open-Circuit Reverse-Voltage Transfer Ratio (Figure 6)	h_{RE}		1.8×10^{-4}	-
Admittance Characteristics:		f = 1MHz, V_{CE} = 3V, I_C = 1mA		
Forward Transfer Admittance (Figure 7)	y_{FE}		31 - j1.5	mS
Input Admittance (Figure 8)	y_{IE}		0.3 + j0.04	mS
Output Admittance (Figure 9)	y_{OE}		0.001 + j0.03	mS
Reverse Transfer Admittance (Figure 10)	y_{RE}		See Figure 10	-
Gain-Bandwidth Product (Figure 11)	f_T	V_{CE} = 3V, I_C = 3mA	550	MHz
Emitter-to-Base Capacitance	C_{EBO}	V_{EB} = 3V, I_E = 0	0.6	pF
Collector-to-Base Capacitance	C_{CBO}	V_{CB} = 3V, I_C = 0	0.58	pF
Collector-to-Substrate Capacitance	C_{CIO}	V_{CI} = 3V, I_C = 0	2.8	pF

Typical Performance Curves

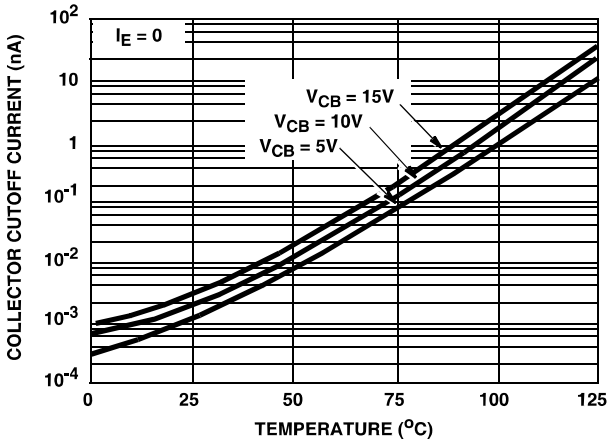


FIGURE 1. I_{CBO} vs TEMPERATURE

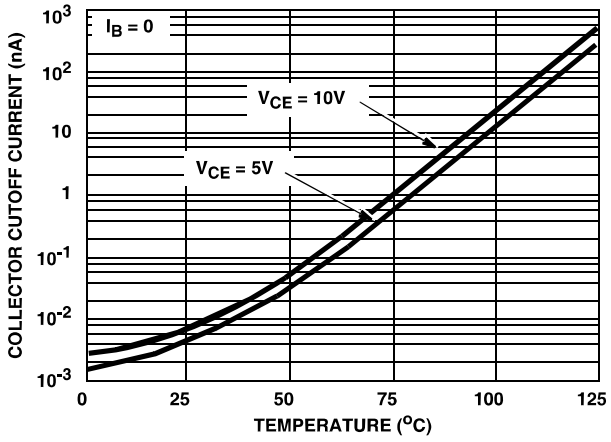


FIGURE 2. I_{CEO} vs TEMPERATURE

Typical Performance Curves (Continued)

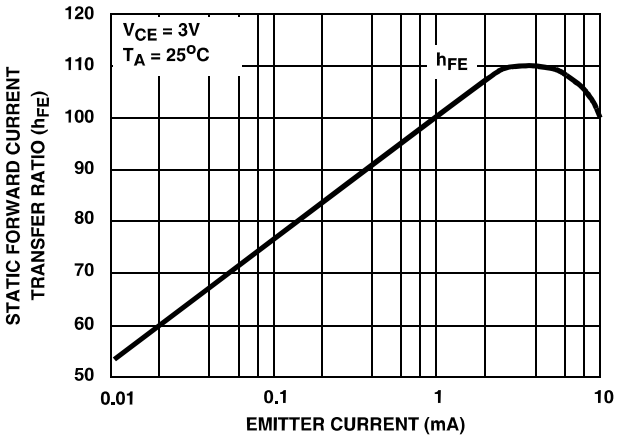


FIGURE 3. h_{FE} vs I_E

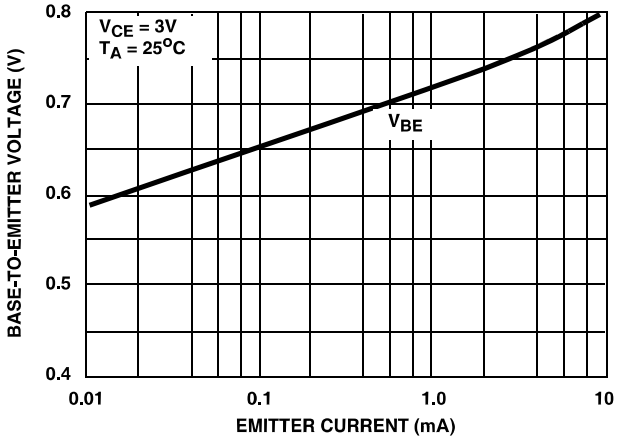


FIGURE 4. V_{BE} vs I_E

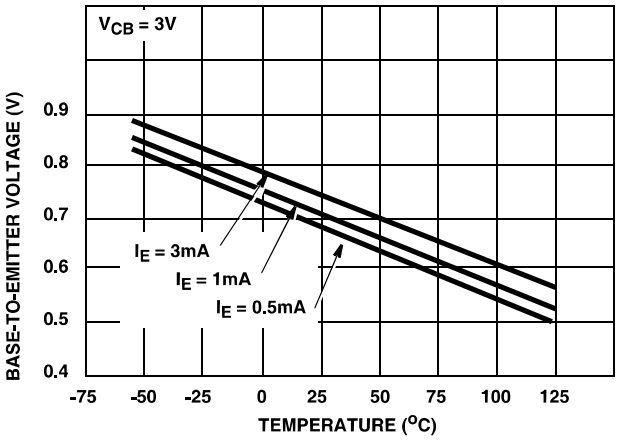


FIGURE 5. V_{BE} vs TEMPERATURE

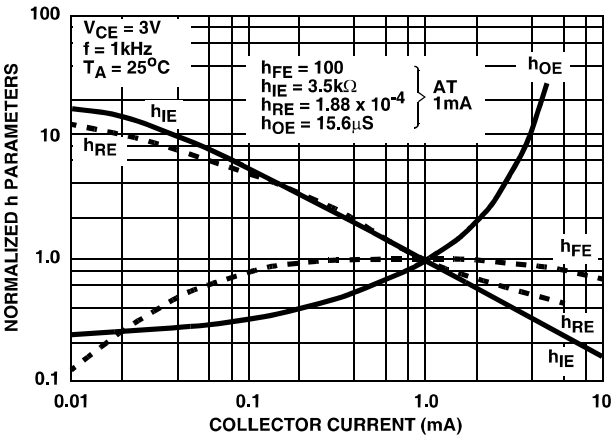


FIGURE 6. NORMALIZED h_{FE}, h_{IE}, h_{RE}, h_{OE} vs I_C

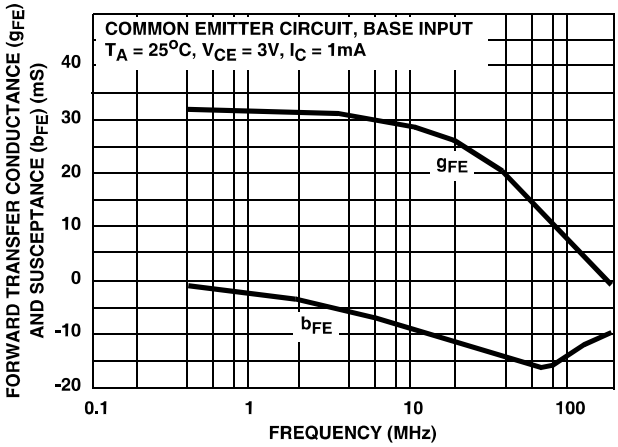


FIGURE 7. y_{FE} vs FREQUENCY

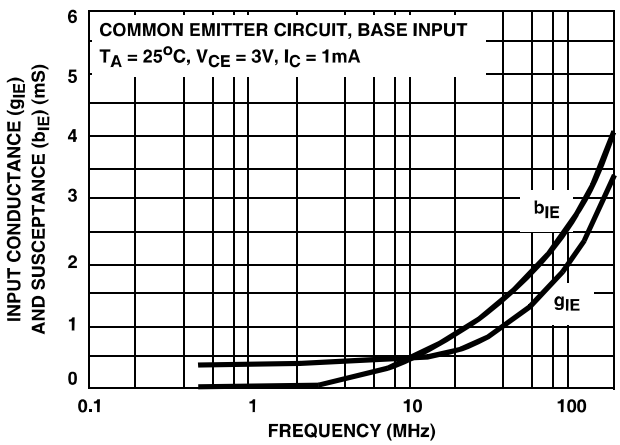


FIGURE 8. y_{IE} vs FREQUENCY

Typical Performance Curves (Continued)

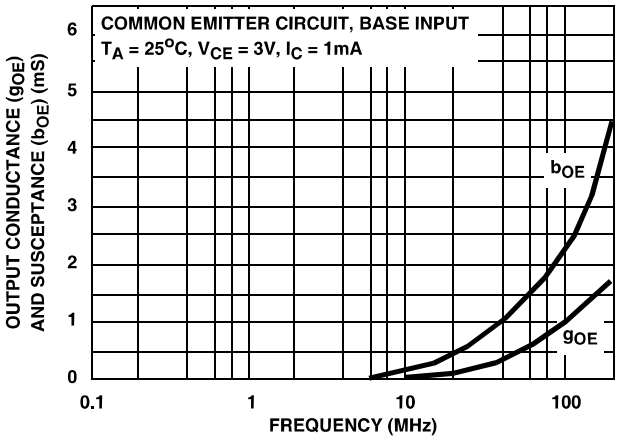


FIGURE 9. y_{OE} vs FREQUENCY

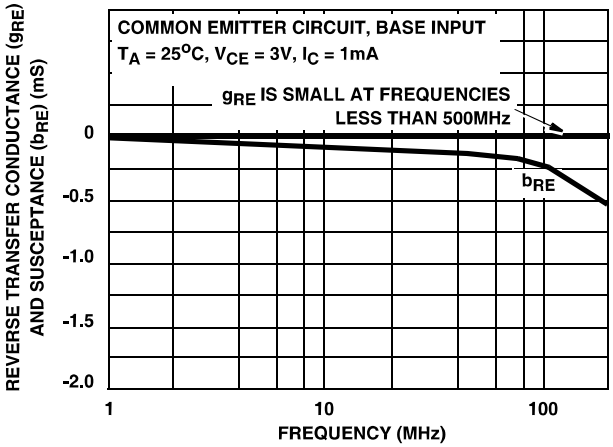


FIGURE 10. y_{RE} vs FREQUENCY

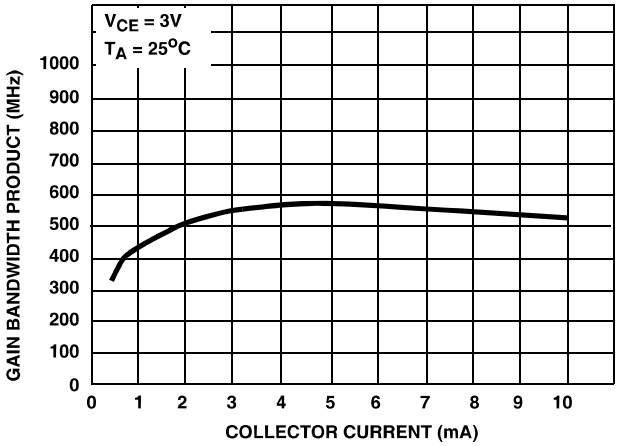
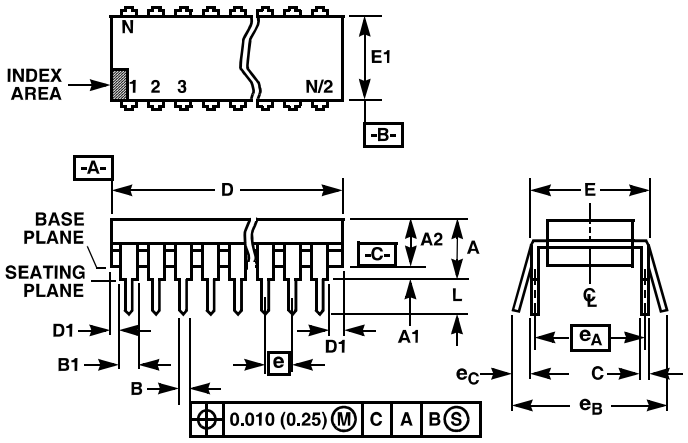


FIGURE 11. f_T vs I_C

Dual-In-Line Plastic Packages (PDIP)



NOTES:

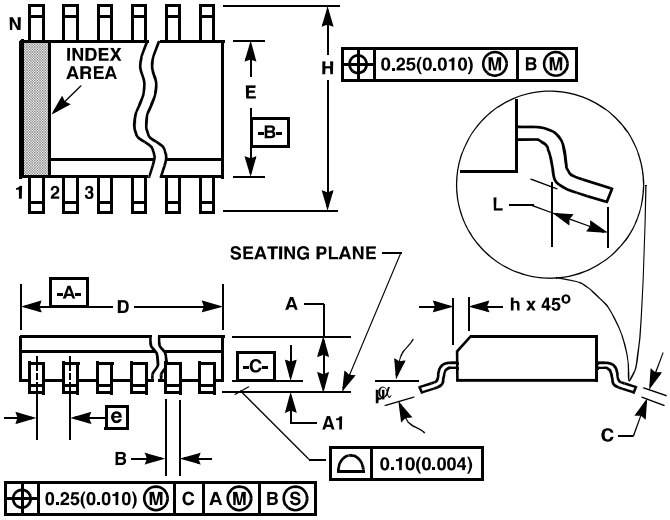
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E14.3 (JEDEC MS-001-AA ISSUE D)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

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Small Outline Plastic Packages (SOIC)



M14.15 (JEDEC MS-012-AB ISSUE C)
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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